IN THE CLAIMS:

Please amend claims 14 and 30, as set forth in the listing of claims provided below:

Claim 1 (previously amended) A logic board designed for circuit emulation, comprising

a plurality of input/output (I/0) pins;

a plurality of emulation integrated circuits (IC), each having reconfigurable logic and interconnect resources reconfigurable to emulate circuit elements of a partition of an IC design; and

a plurality of on-board data processing resources coupled to said emulation ICs to locally retrieve from said emulation ICs state data of emulated circuit elements, responsive to a monitor and report request received through said I/O pins, and to locally analyze the retrieved state data to detect occurrence of one or more events, as well as report on the occurrence of the one or more events upon their detection through said I/O pins;

wherein the on-board data processing resources are further employed to locally generate a plurality of testing stimuli, and locally apply said locally generated testing stimuli to emulation circuit elements of a respective emulation IC corresponding to said partition of the IC design being emulated, responsive to a testing request received through said I/O pins, and wherein at least one of said emulation ICs comprises on-chip programmable data processing resources to cooperate with and assist said onboard data processing resources to perform said local generation and application of testing stimuli.

Claim 2 (previously amended) The logic board as set forth in claim 1, wherein the on-board data processing resources comprise a storage medium having stored therein programming instructions designed to operate the logic board to perform said responsive local retrieval of state data of the emulated circuit elements, local analysis of the retrieved state data, and reporting of event detection, and a processor coupled to the storage medium to execute the programming instructions.

Claim 3 (original) The logic board as set forth in claim 1, wherein at least one of said emulation ICs comprises on-chip data processing resources to cooperate and assist said on board data processing resources to perform said local monitoring and reporting of monitored events.

Claim 4 (cancelled)

Claim 5 (previously amended) The logic board as set forth in claim 1, wherein the on-board data processing resources comprise a storage medium having stored therein programming instructions designed to operate the logic board to perform said responsive local generation and application of stimuli, and a processor coupled to the storage medium to execute the programming instructions.

Claim 6 (cancelled)

Claim 7 (previously amended) In an emulation apparatus, a method of operation comprising:

receiving by an emulation logic board, through input/output (I/O) pins of said logic

board, a monitor and report request;

in response, locally retrieving from emulation ICs of said logic board state data of emulated circuit elements of a partition of an IC design being emulated;

locally analyzing said retrieved state data to detect occurrence of one or more events; and

reporting through said I/O pins of said logic board occurrence of said one or more events, upon detection of their occurrence;

wherein the method further comprises locally generating on said logic board a plurality of testing stimuli, and applying said locally generated testing stimuli to emulation circuit elements of a respective emulation IC corresponding to said partition of the IC design being emulated, responsive to an external testing request received by said logic board through said I/O pins of the logic board, and wherein at least some of said generation of testing stimuli are performed by on-chip programmable data processing resources of said emulation ICs.

Claim 8 (original) The method as set forth in claim 7, wherein at least some of said analysis and detection are performed by on-chip data processing resources of said emulation ICs, in lieu of retrieving the state data from the emulation ICs and then analyzing the state data to detect for the one or more events.

Claims 9-10 (cancelled)

Claim 11 (previously amended) A logic board designed for circuit emulation, comprising

a plurality of input/output (I/O) pins;

a plurality of emulation integrated circuits (IC), each having reconfigurable logic and

interconnect resources reconfigurable to emulate circuit elements of a partition of an IC design; and

a plurality of on-board data processing resources coupled to said emulation ICs to locally generate a plurality of testing stimuli, and locally apply said locally generated testing stimuli to emulated circuit elements of a respective emulation IC corresponding to said partition of the IC design being emulated, responsive to an external testing request received through said I/O pins;

wherein at least one of said emulation ICs comprises on-chip programmable data processing resources to cooperate with and assist said on-board data processing resources to perform said local generation and application of testing stimuli.

Claim 12 (original) The logic board as set forth in claim 11, wherein the on-board data processing resources comprise a storage medium having stored therein programming instructions designed to operate the logic board to perform said responsive local generation and application of stimuli, and a processor coupled to the storage medium to execute the programming instructions.

Claim 13 (cancelled)

Claim 14 (currently amended) In an emulation apparatus, a method of operation comprising:

receiving by a logic board, through input/output (I/O) pins of said logic board, a testing request;

in response, locally generating on said logic board a plurality testing stimuli;

and

locally applying said locally generated testing stimuli to emulation circuit elements of an emulation IC corresponding to a partition of an IC design being emulated;

wherein at least some of said generation of testing stimuli are performed by on-chip programmable data processing resources of said emulation ICs;

~~wherein at least some of said generation of testing stimuli are performed by on-chip data processing resources of said emulation ICs~~.

Claims 15-18 (cancelled)

Claim 19 (previously amended) An emulation system comprising:

a plurality of logic boards, each having a plurality of emulation integrated circuits (IC) including reconfigurable logic and interconnect resources reconfigurable to emulate circuit elements of a respective emulation IC corresponding to a respective one of partitions of an IC design, and on-board data processing resources to locally and correspondingly generate testing stimuli, and apply the generated stimuli to the emulated circuit elements of a respective emulation IC corresponding to a respective one of the partitions of the IC design being emulated, responsive to testing requests received through input/output (I/O) pins of the logic boards; and

a workstation coupled to the logic board, including electronic design automation (EDA) software to provide said logic boards with said testing requests;

wherein at least one of said emulation ICs of said logic boards comprises on-chip programmable data processing resources to cooperate with and assist the on-board data processing resources of the logic board to perform said local and corresponding generation and application of testing stimuli.

Claim 20 (original) The emulation system as set forth in claim 19, wherein the on-board data processing resources of each of the logic board comprise storage medium having stored therein programming instructions designed to operate the logic board to perform said local and corresponding generation and application of testing stimuli.

Claims 21-23 (cancelled)

Claim 24 (previously amended) In an emulation system, a method of operation comprising:

locally and correspondingly generating testing stimuli; and

locally and corresponding applying the generated testing stimuli to selected ones of the emulation circuit elements of emulation ICs corresponding to respective partitions of an IC design being emulated;

wherein at least some of said performances of local and corresponding generation and application of testing stimuli are assisted by on-chip programmable data processing resources of the emulation ICs of the logic boards.

Claim 25 (cancelled)

Claims 25-29 (cancelled)

Claim 30 (currently amended) In an emulation integrated circuit (IC), a method of operation comprising:

locally retrieving on said emulation IC, using on-chip data processing resources, state data of emulated circuit elements of the emulation IC corresponding to a partition of an IC design being emulated;

locally analyzing said state data of the ~~emulation~~ emulated state circuit elements, using on chip data processing resources, to detect occurrence of one or more events; and

reporting on occurrence of said one or more events upon detecting their occurrence;

wherein the method further comprises

locally generating testing stimuli using said on-chip programmable data processing resources; and

locally applying the generated testing stimuli to an IC design being emulated, using said on-chip data processing resources.

Claim 31 (cancelled)

Claim 32 (previously amended) An emulation integrated circuit (IC) comprising:

a plurality of reconfigurable logic and interconnect resources configured to form emulated circuit elements corresponding to a partition of an IC design being emulated; and

programmable on-chip data processing resources coupled to said reconfigurable logic and interconnect resources to locally generate testing stimuli, and locally apply the generated testing stimuli to at least one of said emulated circuit elements.

Claim 33 (previously amended) The emulation IC as set forth in claim 32, wherein said on-chip data processing resources comprise a storage medium having stored therein programming

instructions designed to perform said local generation and application of testing stimuli.

Claim 34 (previously amended) In an emulation integrated circuit (IC) comprising a plurality of reconfigurable logic and interconnect resources configured to form emulated circuit elements corresponding to a partition of an IC design being emulated, a method of operation comprising:

locally generating on said emulation IC testing stimuli, using programmable on-chip data processing resources; and

locally applying the testing stimuli, using said programmable on-chip data processing resources, to at least one of said emulated circuit elements.